

FIG. 1
PRIOR ART

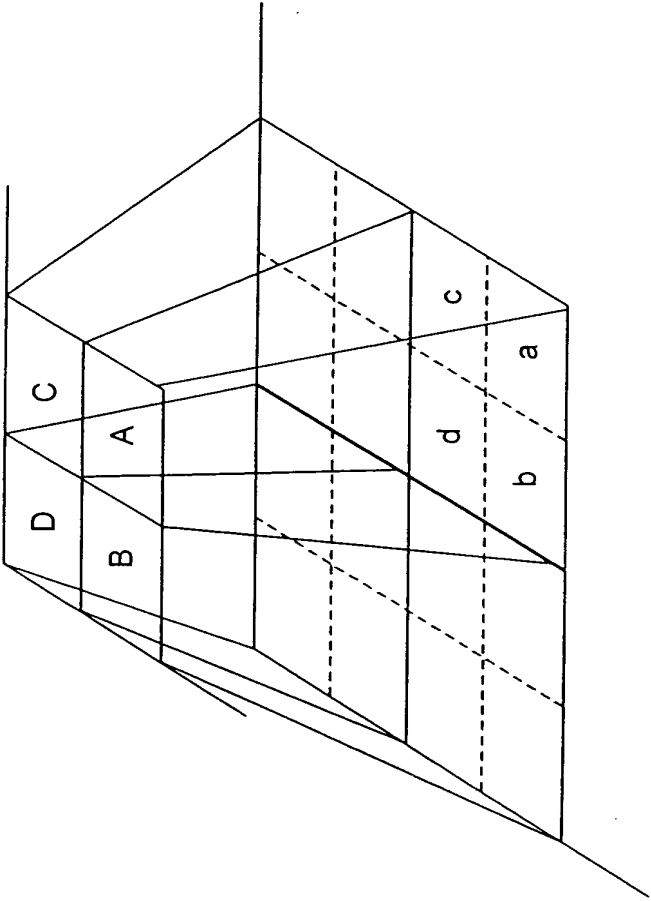


FIG. 2

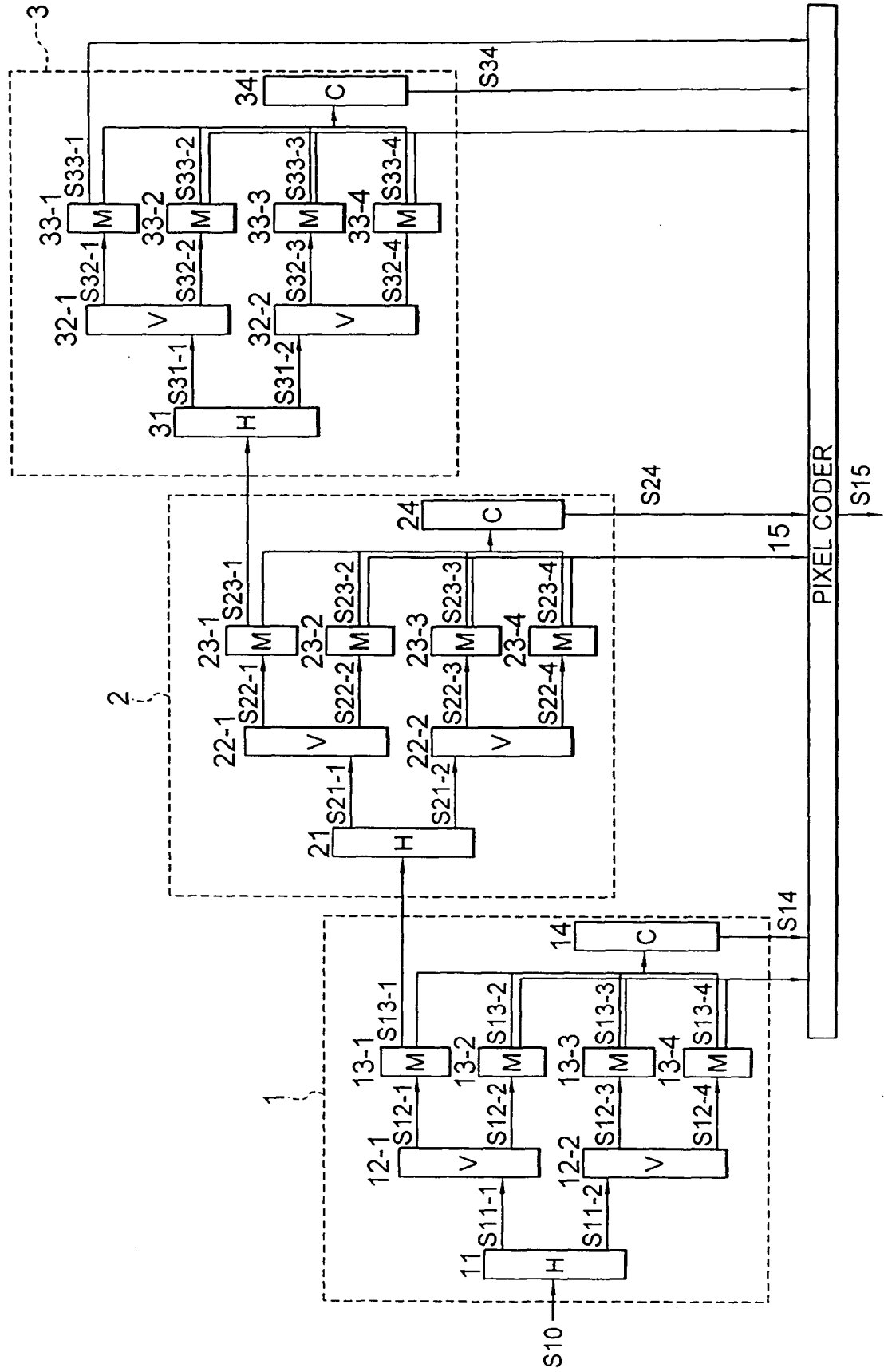


FIG. 3

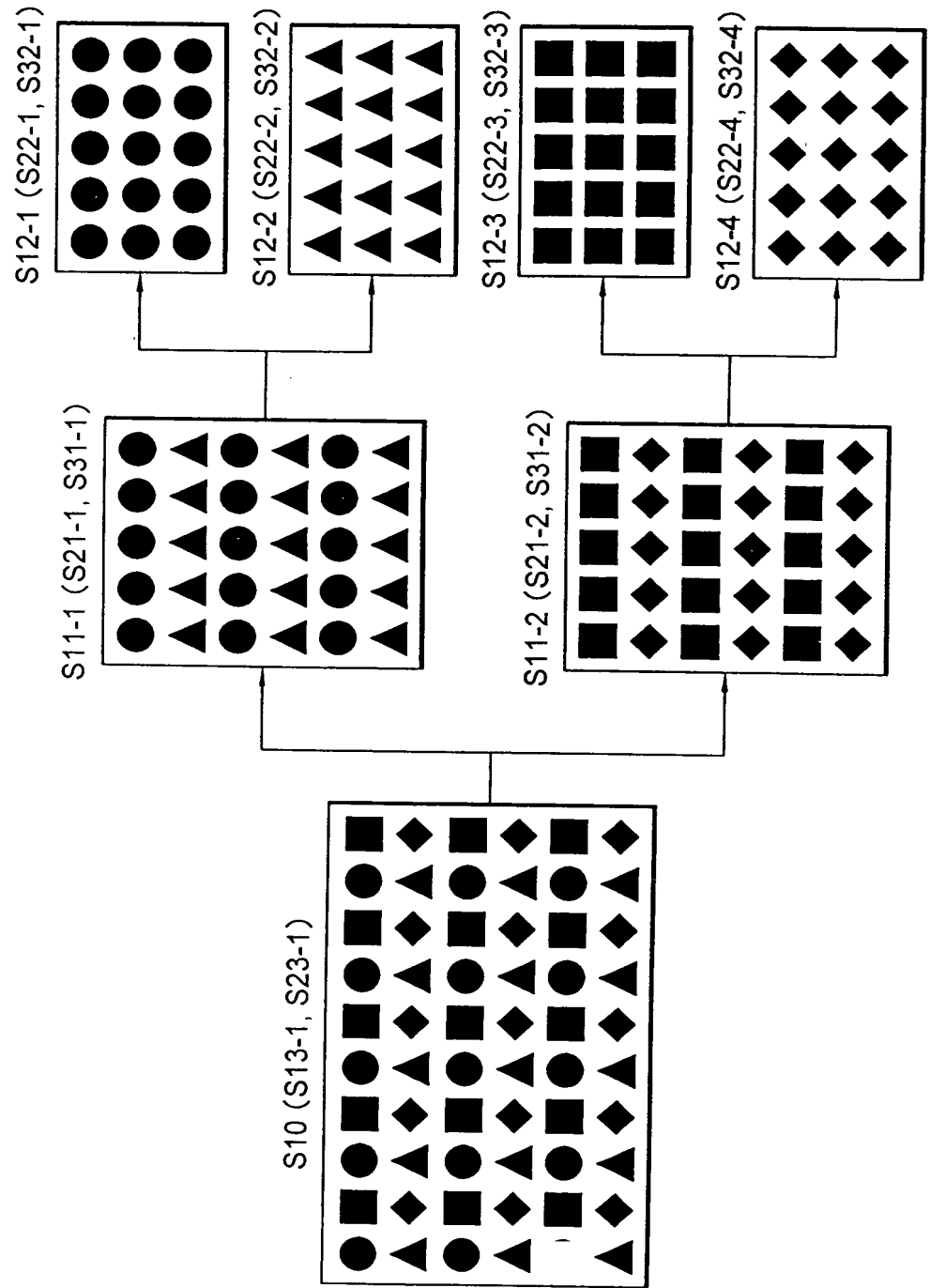


FIG. 4

	I	II	III	IV
1ST MEMORY				
2ND MEMORY				
3RD MEMORY				
4TH MEMORY				

FIG. 5

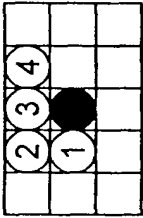
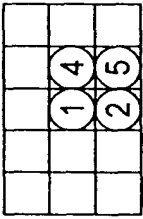
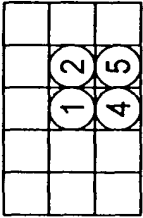
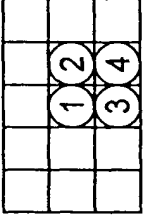
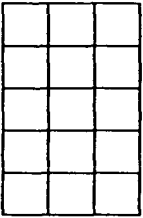
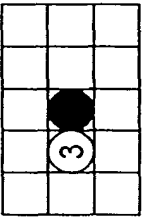
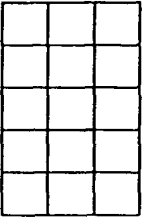
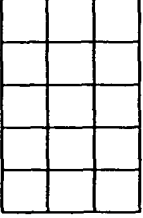
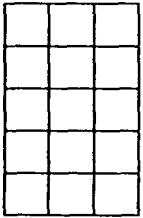
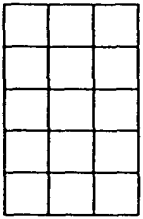
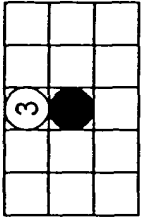
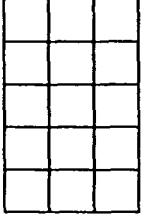
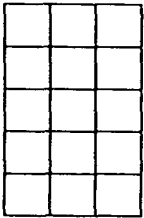
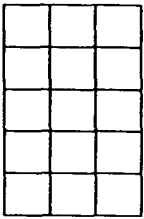
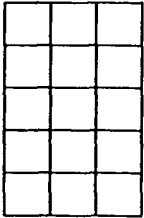
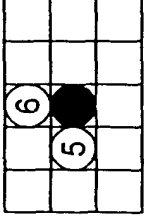
	I	II	III	IV
1ST MEMORY				
2ND MEMORY				
3RD MEMORY				
4TH MEMORY				

FIG. 6

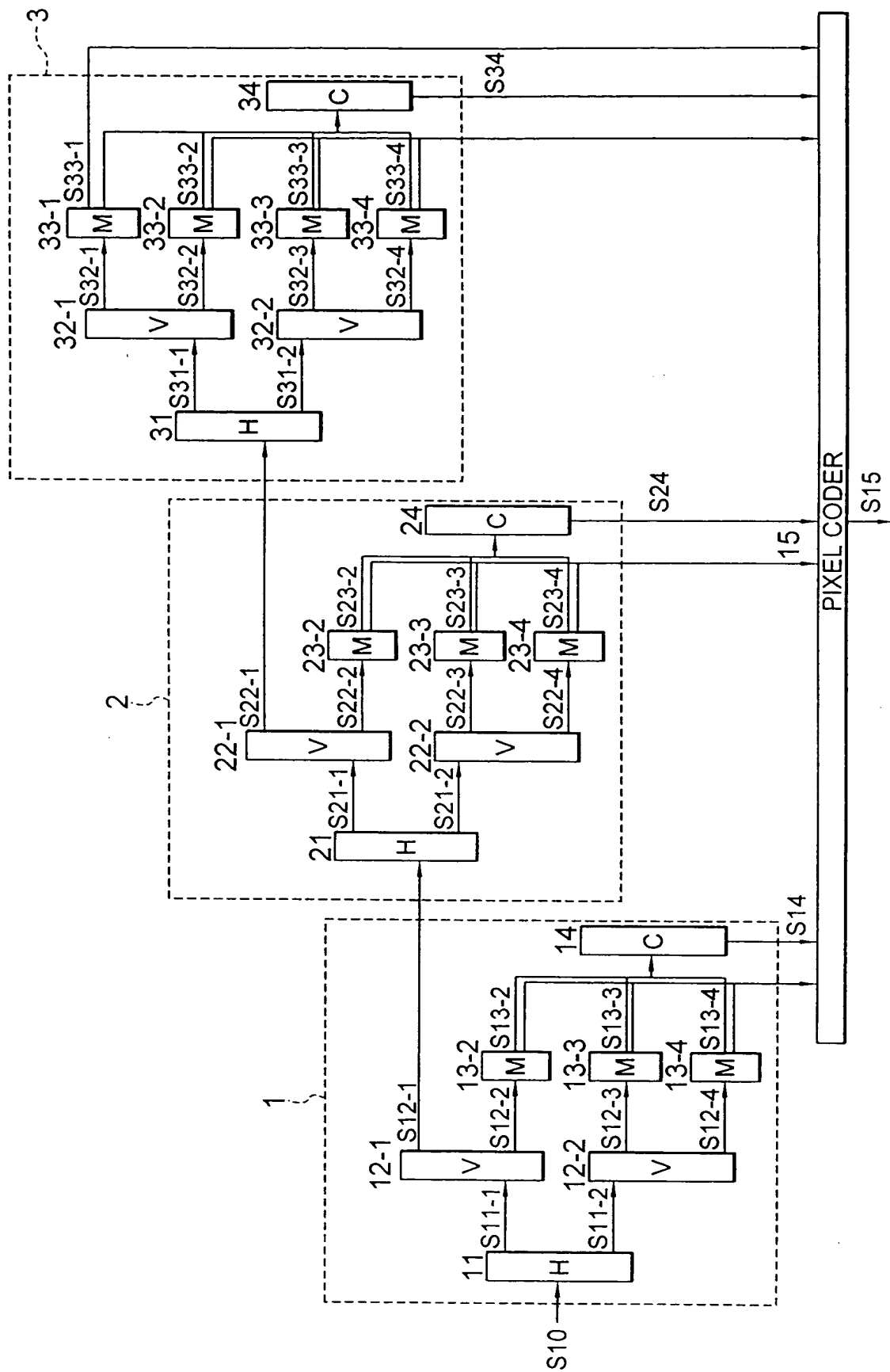


FIG. 7

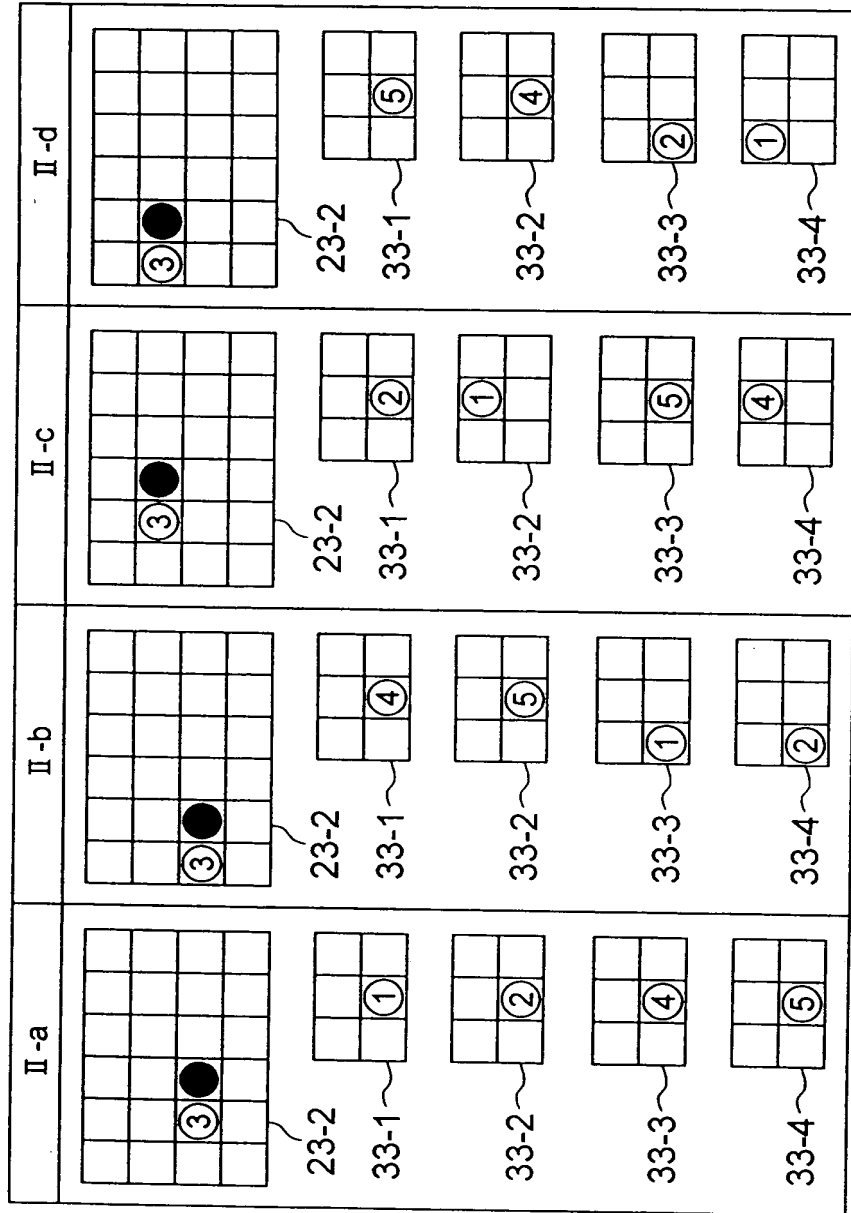


FIG. 8

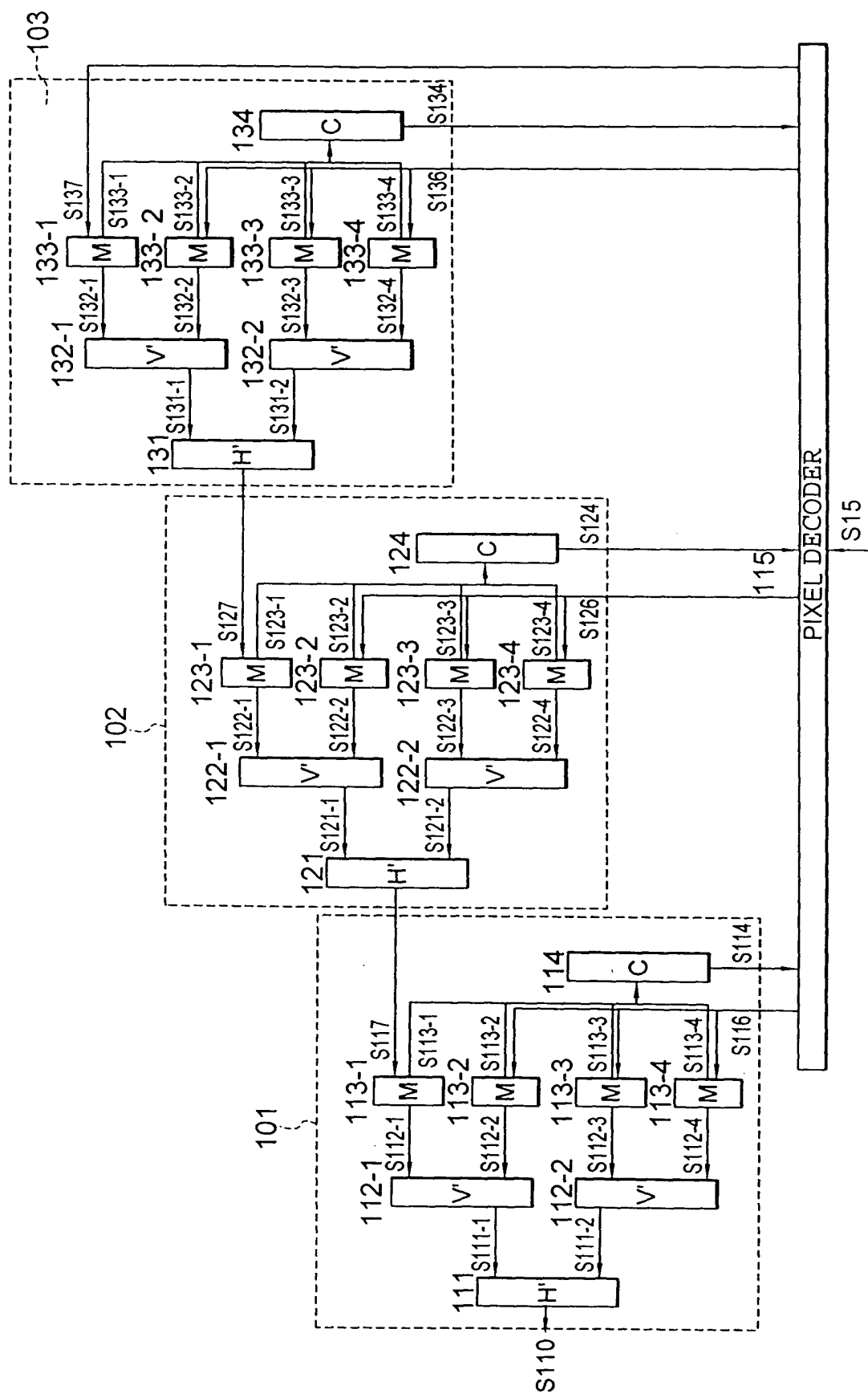


FIG. 9

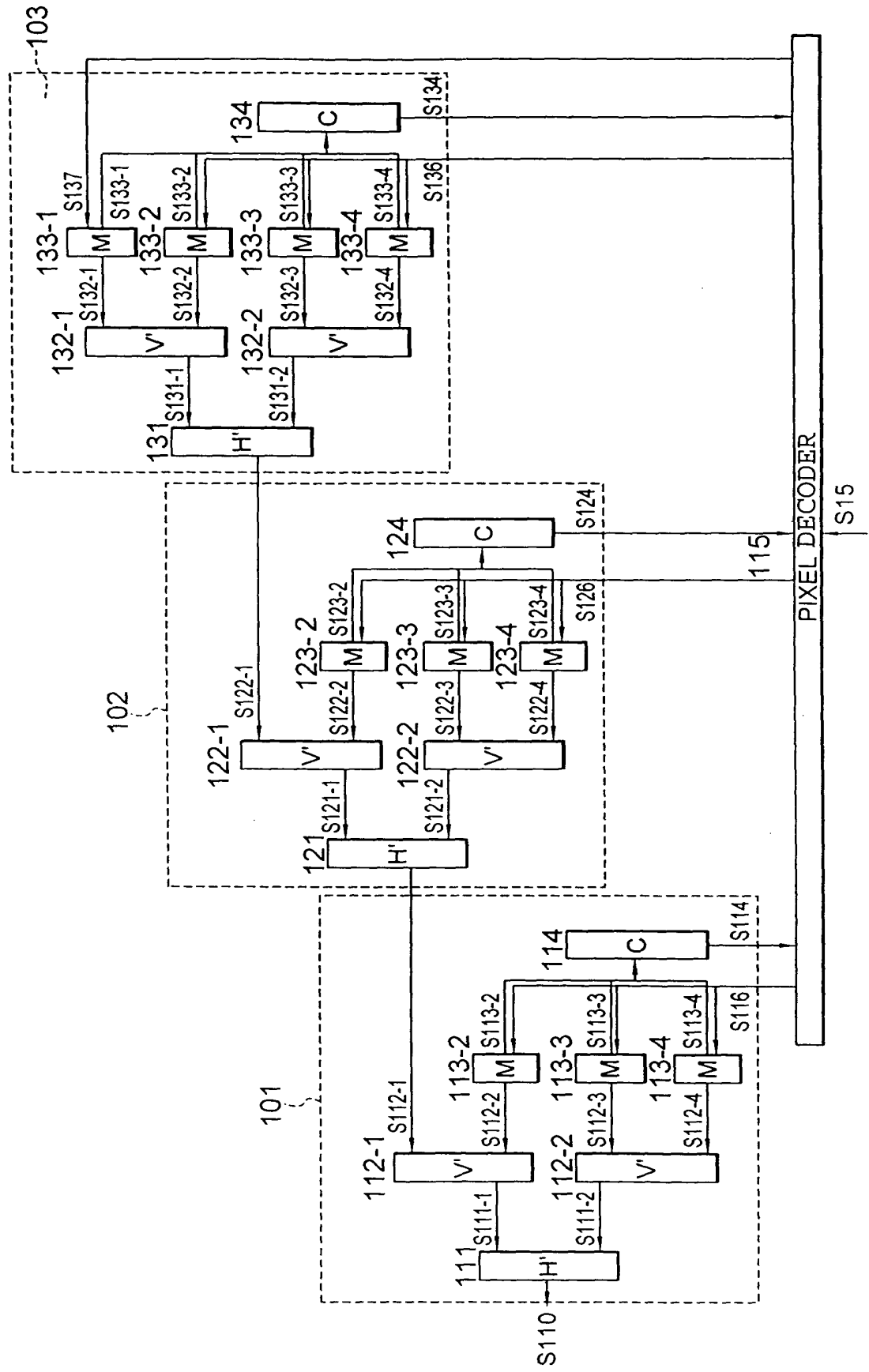


FIG. 10

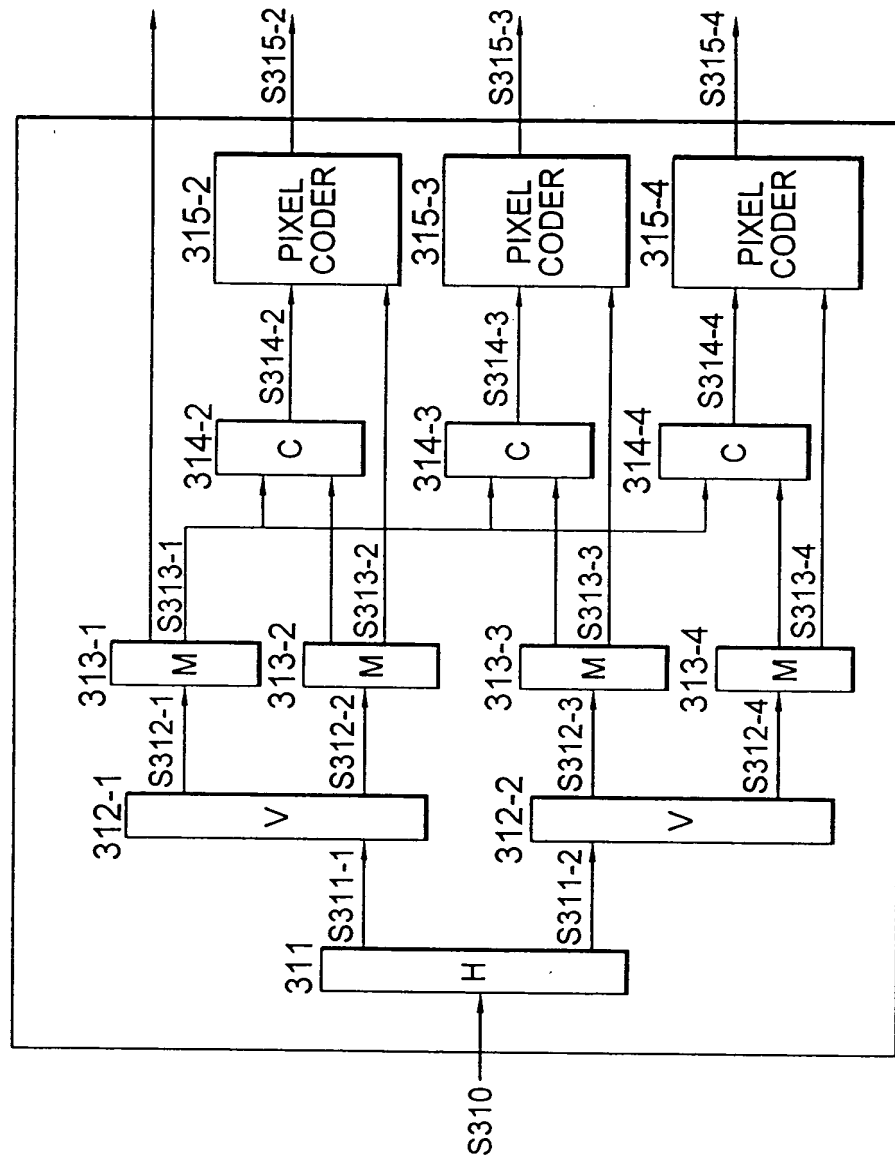


FIG. 11

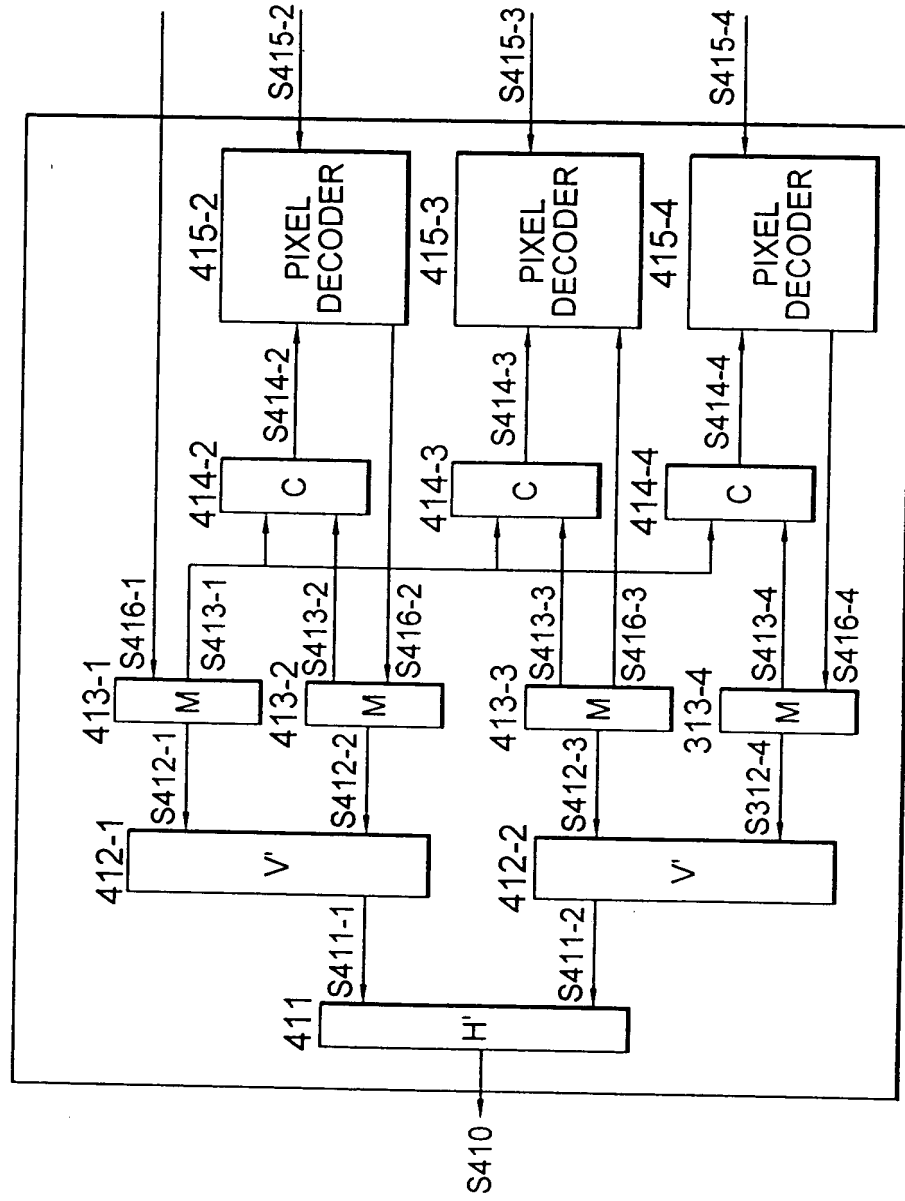
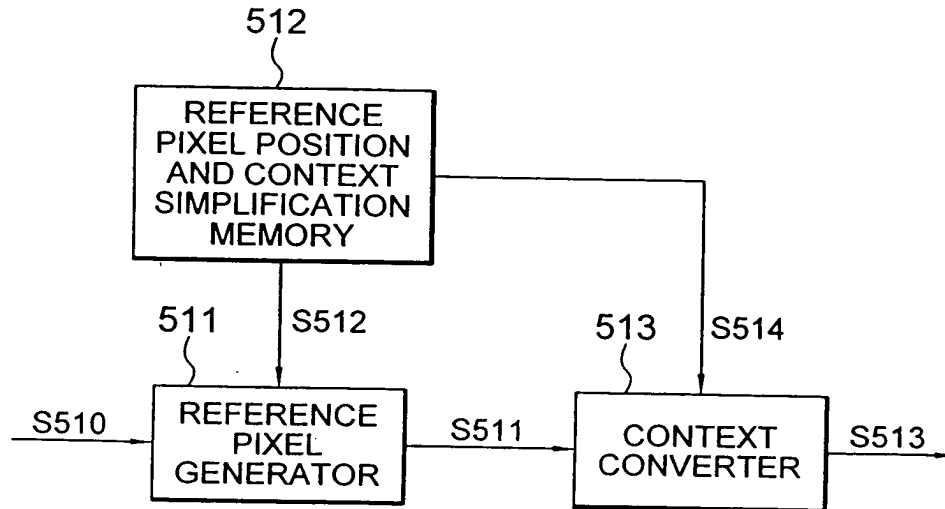


FIG. 12

FIG. 13
PRIOR ART